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Attorney's Docket No.: 10559-595001/P12879

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al.
Serial No.: 09/942,102
Filed : August 29, 2001
Assignee : Intel Corporation
Title : GENERATING A LOGIC DESIGN

Art Unit: 2825
Examiner: Annette M.
Thompson

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information
Disclosure Statement and documents listed on form PTO-1449.

Copies of the U.S. patents and publications are not being
provided per the waiver posted on the PTO website.

Kindly accept this Information Disclosure Statement under
Rule 97(c)(2). The rule 17(p) certification fee of \$180 is
enclosed.

The documents are in the English language; hence no concise
explanation is necessary per Rule 98(a)(3).

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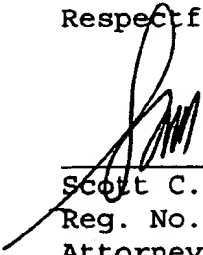
Attorney's Docket No.: 10559-595001

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 3/24/04



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Substitute Form PTO-1449

U.S. Department of Commerce
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Attorney's Docket No.

10559-595001

Application No.

09/942,102

Information Disclosure Statement
by Applicant

(Use several sheets if necessary)

Applicant

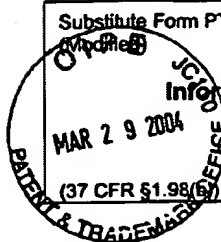
William R. Wheeler et al.

Filing Date

August 29, 2001

Group Art Unit

2825

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
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EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	6,216,256	04/2001	Inoue, et al.			
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	ABBB	2003/0004699	01/2003	Choi, et al.			

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Substitute Disclosure Form (PTO-1449)

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-595001	Application No. 09/942,102
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al.	
		Filing Date August 29, 2001	Group Art Unit 2825

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ACCC	2003/0036871	02/2003	Fuller, et al.			
	ADDD	2003/0177455	09/2003	Kaufman, et al.			

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AEEE	0 404 482	12/1990	EPO				
	AFFF	0 720 233	07/1996	EPO				
*	AGGG	0 901 088	03/1999	EPO				
	AHHH	58-060559	04/1983	Japan				
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*	ANNN	WO 99/39268	08/1999	WIPO				
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	AQQQ	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
	ARRR	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
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	ATTT	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", <i>Electrical Design News</i> , 41(14):129-136 (1996).
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Other Documents (Include Author, Title, Date, and Place of Publication)

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	AVVV	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
	AWWW	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
	AXXX	NN9407481, "Functional Modeling using object Collaboration Diagram", IBM Technical Disclosure Bulletin, Vol. 37, No. 7, July 1994, pp. 481-486.
	AYYY	Parlakbilek, et al., "A Multiple-Strength Multiple-Delay Compiled-Code Logic Simulator", <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 12(12):1937-1946 (1993).
	AZZZ	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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